2811

DOCKET NO.: S01022.80385.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Antonio Torres, et al.
Serial No:	09/497,916
Filed:	February 4, 2000
For:	AN INTEGRATED CIRCUIT INCLUDING PROTECTION AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL
Confirmation. No.:	8061
Examiner:	O. Nadav
Art Unit:	2811

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on the 22nd day of January, 2003.

Signature

Commissioner For Patents
Washington, D.C. 20231

Sir:

Transmitted herewith are the following documents:

[X] Amendment
[X] Return Receipt Postcard

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned at (617) 720-3500, Boston, Massachusetts.

A check is not enclosed. If a fee is required, the Commissioner is hereby authorized to charge Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

Respectfully submitted,
Antonio Torres, et al., Applicant

By: _____
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Docket No. S01022.80385.US
Date: January 22, 2003
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ATTORNEY'S DOCKET NO: S01022.80385.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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3-25-03
Payton

Applicant:	Antonio Torres et al.
Serial No:	09/497,916
Filed:	February 4, 2000
For:	An Integrated Circuit Including Protection Against Polarity Inversion of the Substrate Potential
Confirmation No.:	8061
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Robin Lecesse
Signature

Commissioner for Patents
Washington, D.C. 20231

Sir:

AMENDMENT

In response to the Office Action mailed April 18, 2002, please amend the above-identified application as follows:

Please amend claim 7 as illustrated in the attachment titled "Marked-Up Claim" to read as follows:

7. (Amended) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

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(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

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(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and